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# A New Control Scheme for a Class-D Inverter with Induction Heating Jar Application by Constant Switching Frequency

Won-Suk Choi†, Nam-Ju Park*, Dong-Yun Lee* and Dong-Seok Hyun*

†*Dept. of Electrical Engineering, HanYang University, HaengDang Dong, SungDong Gu, 133-791, Seoul, Korea

## ABSTRACT

In this paper, a simple power control scheme for a constant frequency Class-D inverter with a variable duty cycle is proposed. It is more suitable and acceptable for high- frequency induction heating (IH) jar applications. The proposed control scheme has the advantages of not only wide power regulation range but also ease of control output power. Also it can achieve a stable and efficient Zero-Voltage-Switching (ZVS) in a whole load range. The control principles of the proposed method are described in detail and its validity is verified through simulated and experimental results on 42.8kHz IGBT for induction heating rated on 1.6kW with constant frequency variable power.

**Keywords:** IH-Jar(Induction Heating-Jar), PFM(Pulse Frequency Modulation), PWM(Power Width Modulation), Class-D Inverter, ZVS(Zero-Voltage-Switching)

## 1. Introduction

Recently with the development of power semiconductor devices, new circuit techniques and control schemes, research on high frequency circuits and advanced power devices such as MOSFETs and IGBTs etc. have been many performed for high power applications [1]-[15]. The various resonant inverters using power devices such as MOSFETs and IGBTs offer reduced switching loss by using soft-switching technique and offer attractive possibilities in developing higher frequencies of operation, higher efficiency, a smaller size and lighter weight. Induction heating (IH) has been a part of high power applications and widely used in industrial fields, office automation fields and electric home appliances. In particular, IH-Jar, which is an application of IH is used in home appliances such as cookers [3]-[5].

The requirements for IH applications are as follows:

- High frequency switching
- High efficiency
- Power factor close to unity
- Low cost
- Wide load range
- Reliability

High-frequency Class-D inverters have become very popular and become more and more widely used in various applications. It must be effectively selected according to the application in order to meet the inverter requirements under a high frequency switching operation due to load specifications. An important goal of power control is to achieve an efficient and useful product. Generally, most induction heating applications use a variable frequency scheme to control output power [5]-[6]. The frequency modulation control is a basic method that is applied against the variation of load or line frequency.

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†Corresponding Author: coffeefull@ihanyang.ac.kr
Tel: +82-2-2290-0341, Fax: +81-2-2297-1569, Hanyang Univ.
*Dept. of Electrical and Electronics Eng., Hanyang Univ.

However, pulse frequency modulation control causes many problems since the switching frequency has to be varied over a wide range to accommodate the worst combinations of load and line. The major disadvantage of this method is the large frequency range required for output power control over a wide range. For operations below resonance, filter components are large because they must be designed for the low frequency range. For operations above resonance, fast switching devices are required to maintain control at the upper frequency range. It is apt to produce audible noise when two or more inverters are operated at the same time with different switching frequency. Besides, the soft switching operating area of the ZVS-PFM high frequency inverter is relatively narrow under a pulse frequency modulation strategy. Keeping the switching frequency constant and controlling it by pulse width modulation (PWM) are obvious ways to avoid the problems of variable frequency control [7]-[11]. Therefore, Class-D inverter topologies using a PWM chopper at the input, phase-shifted PWM control, PWM technique, current mode control and a variable resonant inductor or capacitor have been proposed. Constant-switching frequency operation supposes that every inverter in the application is operating at the same frequency, making it necessary to control power without frequency variations. That is highly desired for optimum design of the output smoothing and noise filters. However these control requirements and operating characteristics have an added complexity due to the fixed frequency of switching which limits their performance [12]. And if the system has a phase-shift PWM control, the ZVS does not exist at light load [13]-[14]. This paper deals with a simple power control scheme of constant frequency variable power (CFVP) for a Class-D inverter with induction heating jar application. When the inverter operates at a fixed switching frequency higher than its resonant frequency, it can maintain the ZVS operation in the whole load range. Thus switching losses, EMI, are decreased. By adjusting the duty cycle of the fixed frequency, the output power is simply controlled in wide load range (10%-100% load). The advantages of this inverter control scheme are simple configuration and wide power regulation range. It can improve the power control and elevate control response performance. Also the switches always guarantee zero-voltage-switching (ZVS) from light to full load and the filter is easy to design due to the use of constant switching frequency. The proposed power control scheme and the principles of the Class-D inverter are explained in detail. Theoretical analysis, simulation and experimental results verify the validity of the Class-D inverter with the proposed PWM control scheme.

## 2. Class-D Series Resonant Inverter [1]

### 2.1 Circuit description

The Class-D inverter will be generally used to energize the induction coil to generate high-frequency magnetic induction between the coil and the cooking vessel, high-frequency eddy currents and finally heat in the vessel bottom area. Class-D inverters take the energy from the mains voltage. The DC voltage is converted again into a high-frequency AC voltage by a Class-D inverter. Then the inverter supplies the high-frequency current to the induction coil.

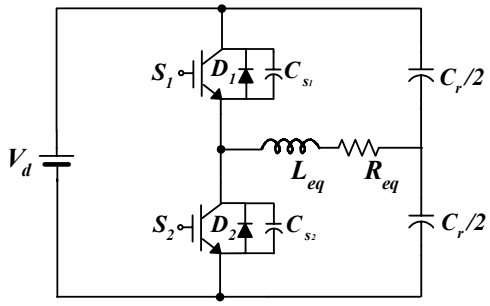



Fig. 1 Class-D inverter system for IH jar application

Fig. 1 shows a Class-D inverter system for a induction heating jar. The Class-D inverter consists of two switches $S_1$, $S_2$ with anti-parallel diodes $D_1$, $D_2$ using IGBT, two resonant capacitors $C_r/2$ and an induction coil that consists of a series combination of resistance $R_{eq}$ and inductance $L_{eq}$. One of the main advantages of the half-bridge inverter is low voltage across the switch that is equal to the supply voltage. Thus, compared with other topologies (Class-E, Quasi-resonant inverter etc.) for induction heating applications, it is suited for high-voltage applications [1]. The utility DC input voltage of 311V is directly supplied into an inverter and $S_1$, $D_1$ and $S_2$, $D_2$ are alternately used to administer high frequency current to the induction coil.

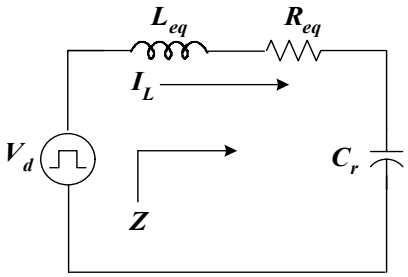



Fig. 2 Equivalent circuit

Fig. 2 represents the equivalent circuit model of a Class-D inverter. In particular, two switches are operated at square wave with suitable dead time between the two driving commands. The Class-D inverter is operated above the resonant frequency, which means that the switches are turned-off while carrying current.

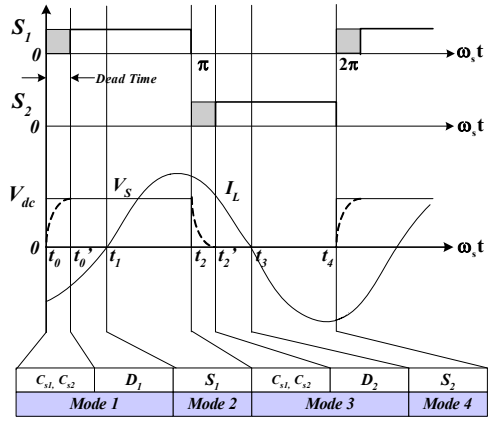



Fig. 3 Theoretical waveforms of the Class-D inverter

Fig. 3 described the operation mode including switching signals and inverter output voltage $V_s$ and current $I_L$ waveforms. As shown in Fig. 3, if the switches are operated above resonant frequency, the series resonant circuit represents an inductive load and the load current $I_L$ lags behind the output voltage $V_s$, Therefore, load current $I_L$ flows in the order of $C_{s1}$,$C_{s2}$→$D_1$→$S_1$→$C_{s1}$,$C_{s2}$→$D_2$→$S_2$. At this time, the switching losses do not occur at turn-on because the switches are turned on at zero voltage. The Class-D inverter with the PWM control scheme is explained in detail when it is applied to the IH-jar.

Fig. 3 and Fig. 4 illustrates the steady-state theoretical waveforms and operation modes of the Class-D inverter. The steady-state analysis of the Class-D inverter is based on the following assumptions.

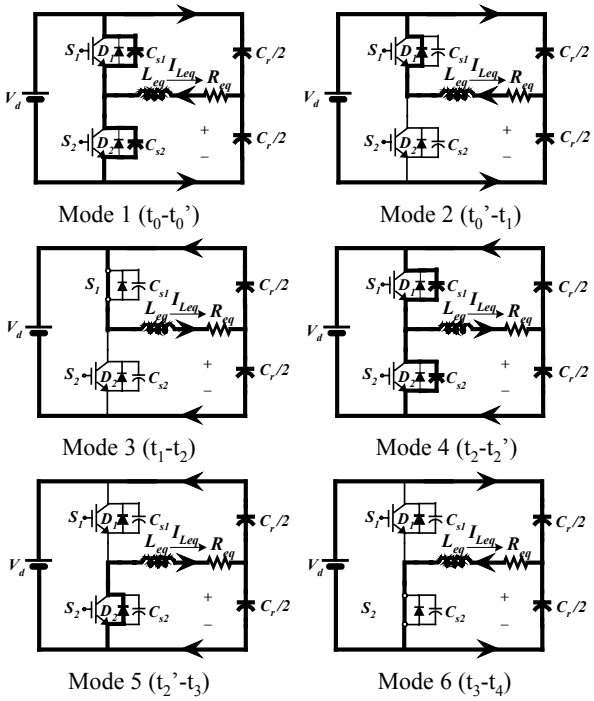



Fig. 4 Operation modes of the Class-D inverter

- All components are ideal.
- Input voltage of the DC link is constant in one switching cycle.
- Effects of the parasitic capacitances of the switch are neglected.
- Load current is nearly sinusoidal because the large load quality factor (Q) is high enough.

### 2.2 Circuit Operation and Analysis of Mode 1, 2, 3

At $t=t_0$, $C_{s1}$ and $C_{s2}$ begin to resonate with energy in the inductor $L_{eq}$. The load current $i_{Leq}$ is transferred from $S_2$ to capacitor $C_{s1}$ and $C_{s2}$. At $t=t_0'$, the load current, $i_{Leq}$ flows through $L_{eq}$→$D_1$→$V_d$→$R_{eq}$, thus switch $S_1$ is turned on under the ZVS condition at $t_1$. These modes are continuous in circuit operation and provide the same circuit connection with its actual direction of current flow shown in Mode 1, Mode 2 and Mode 3 of Fig. 4. At this point, according to the Thevenin short-open circuit method, the Thevenin impedance $Z_{TH}=1/(2\pi fc)$ and Thevenin voltage $V_{TH}=+V_d/2$ can be obtained. Next, the energy is delivered from input to load side through switch $S_1$ voltage and the current equations of the equivalent circuit are represented by Eq. 1 and Eq. 2 at turn-on.

$$\pm V_d/2 = R_{eq} i_{Leq} + L_{eq}\frac{di_{Leq}}{dt} + \frac{1}{C}\int i_{Leq}\,dt \quad (1)$$

$$i_{L_{eq}} = e^{-\frac{R_{eq}}{L_{eq}}t}\left[ I_1 \cos\beta t_1 + \left( \pm\frac{Vd}{2\beta_{L_{eq}}} - \frac{V_1}{\beta L_{eq}} - \frac{R_{eq}}{2\beta L_{eq}} I_1 \right) \sin\beta t_1 \right] \quad (2)$$

Where

$\beta = \sqrt{(R_{eq}/4L_{eq})^2 - (1/L_{eq}C_r)}$

$V_1$, $I_1$ : Initial Voltage across $C_r$ and current though $L_{eq}$ in the RLC equivalent circuit

$+V_d$ : for Modes 1, 2 ; and $-V_d$ : for Mode 3, 4

### 2.3 Circuit Operation and Analysis of Mode 4, 5, 6

The analysis procedures in these two modes are the same as in the previous ones. The two modes of circuit operation are also continuous and provide the circuit connection as shown in Mode 4, Mode 5 and Mode 6 of Fig. 4. The Thevenin impedance $Z_{TH} = 1/(2\pi fc)$ and Thevenin voltage $V_{TH} = -V_d/2$ are also obtained.

Parameters for analysis include the following.

a) The resonant frequency

$$\omega_r = \frac{1}{\sqrt{L_{eq} \cdot C_r}} \quad (3)$$

The normalized switching frequency

$$\omega_n = \frac{\omega_s}{\omega_r} \quad (4)$$

Fig. 5(a). illustrates (5) in a three-dimensional space as a function of (4), (6)

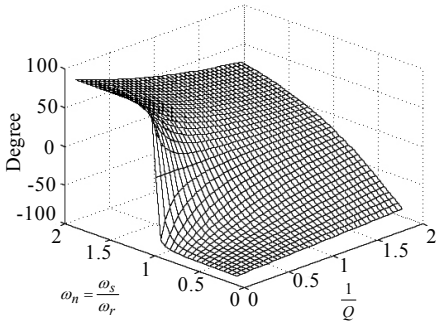
The characteristic impedance

$$Z_0 = \sqrt{\frac{L_{eq}}{C_r}} = \frac{1}{\omega_r C_r} = \omega_r L_{eq} \quad (5)$$

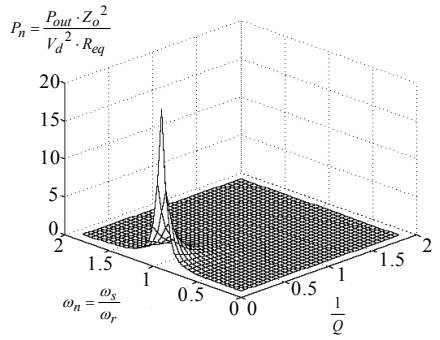
The quality factor

$$Q = \frac{\omega_r \cdot L_{eq}}{R_{eq}} = \frac{1}{\omega_r R_{eq} C_r} = \frac{Z_0}{R_{eq}} \quad (6)$$

The input impedance of the resonant tank circuit in Fig 2.




(a) Characteristic impedance.




(b) Output power $P_{out}$.

Fig. 5 Three-dimensional representation of the , $P_{out}$ as function of and 1/Q

$$Z = R_{eq} + j\left(\omega_s L_{eq} - \frac{1}{\omega_s C_r}\right)$$
$$= R_{eq} \cdot \left(1 + jQ \cdot \left(\omega_n - \frac{1}{\omega_n}\right)\right) \quad (7)$$

$$|z| = R_{eq} \cdot \sqrt{1 + Q^2 \cdot \left(\omega_n - \frac{1}{\omega_n}\right)^2} \quad (8)$$

The current phase angle is

$$\Phi^\circ = \tan^{-1}\left(Q \cdot \left(\omega_n - \frac{1}{\omega_n}\right)\right) \quad (9)$$

The input voltage of resonant tank circuit $V_s$ is

$$V_s = \begin{cases} V_d & for \quad 0 < \omega_s t \le \pi \\ 0 & for \quad \pi < \omega_s t \le 2\pi \end{cases} \quad (10)$$

The fundamental wave of the alternating component of *Vs* can be found by Fourier analysis:

$$V_{s1} = V_m \cdot \sin \omega_s t , \qquad for \quad 0 < \omega_s t \le 2\pi \tag{11}$$

Where

$$V_m = \frac{2 \cdot V_d}{\pi} \approx 0.637 \cdot V_d \tag{12}$$

The load current through the resonant tank circuit is derived by

$$i_L = I_m \cdot \sin(\omega_s t - \Phi) \tag{13}$$

Where

$$I_m = \frac{V_m}{|Z|} = \frac{2 \cdot Vd}{\pi \cdot |Z|} = \frac{2 \cdot V_d \cdot \cos\phi}{\pi \cdot R_{eq}} = \frac{2 \cdot V_d}{\pi \cdot R_{eq} \cdot \sqrt{1 + Q^2 \cdot \left( \omega_n - \frac{1}{\omega_n} \right)^2}} \tag{14}$$

Fig. 5 (b). illustrates (15) in a three-dimensional space as a function of (4), (6)

The conventional output power is given by using Eq (14).

$$P_{out} = I_m{}^{2} \cdot \frac{R_{eq}}{2} = \frac{2 \cdot V_d{}^2 \cdot \cos^2 \phi}{\pi^2 \cdot R_{eq}} = \frac{2 \cdot V_d{}^2}{\pi^2 \cdot R_{eq} \cdot \left( 1 + Q^2 \cdot \left( \omega_n - \frac{1}{\omega_n} \right)^2 \right)} \tag{15}$$

If $\omega_{rated}$ is the switching frequency at full load power, $\omega_s = \omega_{rated}$ , $P_{out}$=$P_{rated}$ at full load power.

We define $D_{power}$ as a ratio of output power and it can be obtain at the low frequency duty ratio $D_{power}$ as a function of $P_{desired} / P_{rated}$.

Therefore, the desired power can be obtained by using Eq (15).

$$P_{desired} = D_{power} P_{rated} = \left\{ I_m{}^{2} \cdot \frac{R_{eq}}{2} \right\} D_{power} = \left\{ \frac{2 \cdot V_d{}^2 \cdot \cos^2 \phi}{\pi^2 \cdot R_{eq}} \right\} D_{power} \tag{16}$$

The desired output power can be regulated by variations of the power control duty ratio, $D_{power}$.

Fig. 6 shows the output power is in proportion to the switching duty cycle in low frequency.

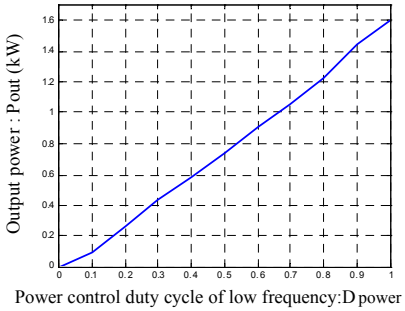



Fig. 6 Output power versus power control duty cycle

Fig. 7 shows the frequency characteristics of the series loaded resonant circuit. The x-axis describes the ratio of the switching frequency to the resonant frequency, and the y-axis describes the normalized power. Switching frequency operates above resonant frequency to ensure a zero-voltage-switching condition. Fig. 8 shows the output power versus the switching frequency with PFM control.

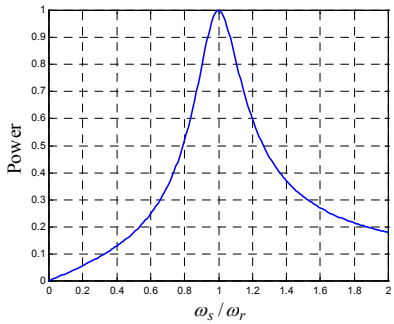



Fig. 7 The frequency characteristics of the series loaded resonant circuit

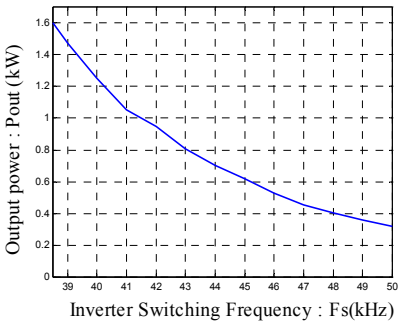



Fig. 8 Output power versus switching frequency

As shown in Fig. 8, the switching frequency is adjusted to generate the desired output power. To obtain maximum power, the switching frequency is very close to the resonant frequency, whereas when low output power is desired for the same load, the switching frequency is farther from the resonant frequency. That is to say, the switching frequency needed for light loads is very high. This increases the magnetic core loss and poses problems in the design of the control circuit and this control scheme requires a wide switching frequency to obtain wide power control range. Therefore the soft switching area is relatively narrow under the PFM strategy.

## 3. Proposed Control Strategy

### 3.1. The Overall Block Diagram

The variable output power is the main value in the Class-D inverter for induction heating jar. We proposed a new simple power control scheme by adjusting the variable duty cycle of the constant low frequency that is combined with a fixed high power frequency. The overall block diagram of the proposed scheme is shown in Fig. 9.

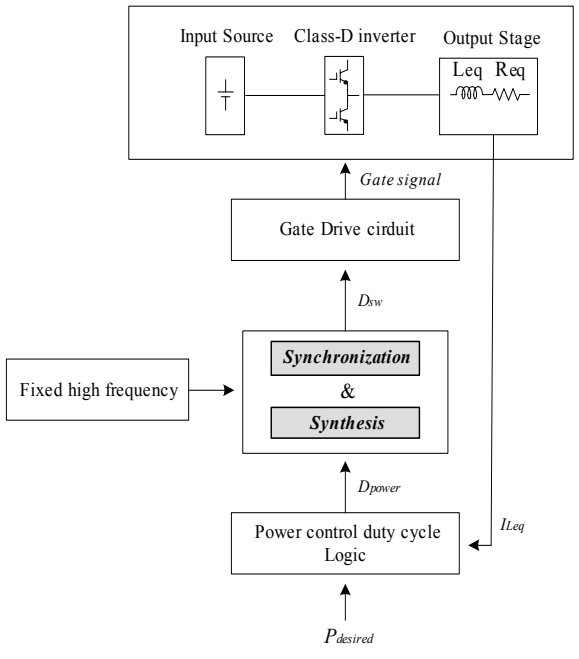



Fig. 9 Proposed Control Block diagram of the Class-D Inverter

The proposed control scheme consists of two parts. One is for controlling the power duty cycle at low frequency, $D_{power,}$ and the other one is for synchronization and synthesis of the fixed low and high frequency signals. The load current, $I_{Leq}$ is compared with the desired power, $P_{desied}$ to decide, $D_{power}$ through the comparator. If $D_{power}$ is decreased, the rms load current, $I_{Leq}$ is also decreased. Therefore, output power can be controlled by adjusting the $D_{power}$ . The $D_{power}$ is synchronized and synthesized with the fixed high frequency. According to the proposed power control scheme, output power is simply controlled by adjusting the $D_{power}$. Since the switches operate at fixed frequency, which is above resonant frequency, switches of this inverter always ensures zero-voltage switching (ZVS) from light to full load. Therefore turn on losses, EMI and noises in the switches are low in the inverter with this proposed control scheme.

### 3.2 The Control Scheme of Synchronizing and Synthesis

To eliminate the current and voltage spikes in on-off times of the low frequency signal, the power control low frequency and constant high frequency signals must be simultaneously crossed zero. The switches $S_1$ and $S_2$ are alternately operated after dead time setting. Fig. 10 shows the control scheme of the synchronization and synthesis logic block.

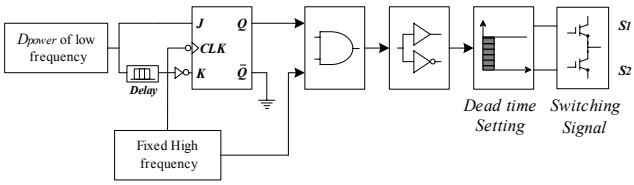



Fig. 10 Control Scheme of the Synchronization and Synthesis Logic Block

The high frequency signal is fixed to a specific value above the determined resonant frequency for zero-voltage-switching. $D_{power}$ is modulated by the feedback load current. These signals have to be synchronized at on-off time by the logic block. The flip-flop is used for synchronization between the fixed low and high frequency signals. As shown in Fig. 11, the two signals are synchronized through the logic and leads to the switching signal $D_{sw}$ , which keeps them synchronized.

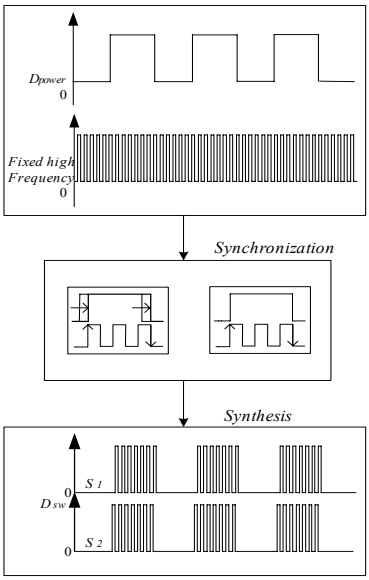



Fig. 11 Waveforms of the Synchronized and Synthesized Signals

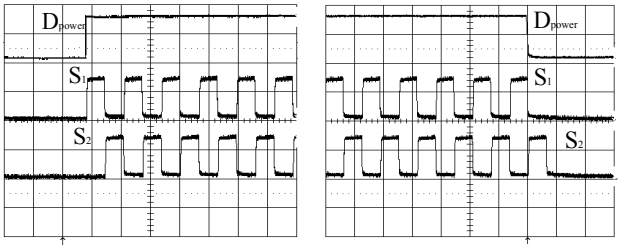
## 4. Simulation And Experimental Results

To verify the validity of the Class-D inverter system with the proposed control scheme, a simulation and an experiment were performed equally under the conditions of Table 1. In addition, Table 1 shows that the switching frequency is greater than the resonant frequency, which means ZVS is achieved.

Table 1 Parameters of the Class-D inverter

| COMPONENTS | | PARAMETERS |
|---|---|---|
| $\mathbf{V_s}$ | Input voltage | 311 $V_{DC}$ |
| $\mathbf{P_{rated}}$ | Rated output power | 1.6kW |
| $\mathbf{f_s}$ | Switching frequency | 42.8kHz |
| $\mathbf{f_p}$ | Power control frequency | 5.4Hz |
| $\mathbf{f_r}$ | Resonant frequency | 34.6kHz |
| $\mathbf{L_{eq}}$ | Equivalent inductor | 66 $\mu$ H |
| $\mathbf{R_{eq}}$ | Equivalent resistor | 6.4Ω |
| $\mathbf{C_r}$ | Resonant capacitor | 320 *n*F |
| $\mathbf{S_1}$, $\mathbf{S_2}$ | Switch | IGBT F90N60UFD |

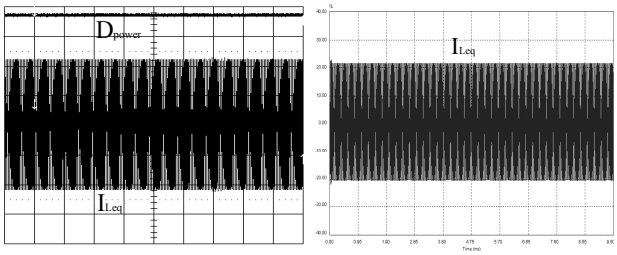
The simulation and experiment results of the Class-D inverter using the proposed scheme are performed in case the system is operated at a variation of load (10%-100%). The constant switching frequency, $f_s$ is chosen as 42.8kHz to generate 1.6kW at full load and we chose the power control frequency, $f_p$ for 5.4Hz to avoid acoustic noise. Fig 12 (a) and (b) show the synchronization between $S_1$ and $S_2$. To eliminate the switching current spike, it must be synchronized between $S_1$ and $S_2$ through a flip-flop at on-off time.




(a). On time of $D_{power}$ (b) Off time of $D_{power}$

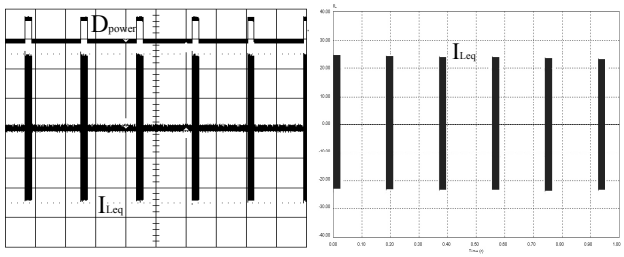
Fig. 12 Synchronized Switching Signal $S_1$, $S_2$, (10V/div., time: 20s)

As shown in Fig 12(a), (b), the power control low frequency, $D_{power}$ and constant high frequency signals simultaneously cross zero at on-off time. Fig. 13(a) shows the simulated and experiment results of the load current $I_{Leq}$ at full load.



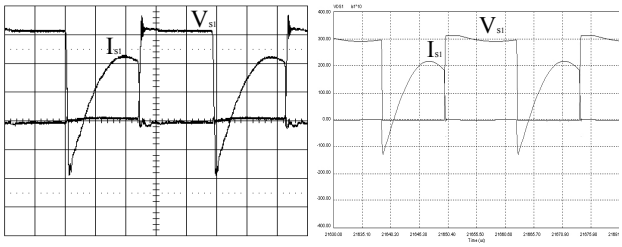

(a) (10A/div., time: 5ms) Load current $I_{Leq}$ at 100% load

As shown in Fig 13(a), the load current $I_{Leq}$ flows continuously due to 100% $D_{power}$. Fig. 13(b) shows the simulated and experiment results of the load current $I_{Leq}$ at 10% load.



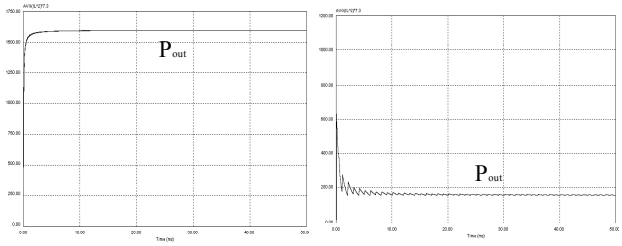

(b) (10A/div., time: 0.1s) Load current $I_{Leq}$ at 10% load

As shown in Fig. 13(b), according to 10% $D_{power}$, the aaverage load current is lower due to the discontinuous flow of $I_{Leq}$, so this means the average output power is deceased. There are no current spikes because switching signals between the high frequency, 42.8kHz and the power control low frequency, $D_{power}$, 5.4Hz are synchronized at on-off time. Fig. 13(c) shows the simulated result of the switch voltage and current at a 10% load.




(c) (100V/div., 10A/div., time: 0.5s)
Switch voltage and current at 10% load

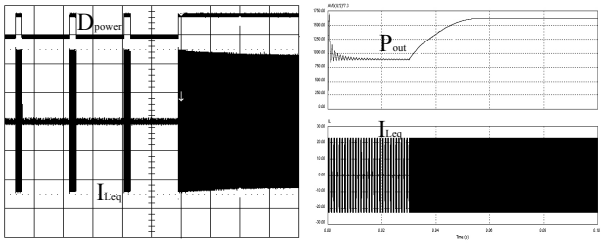
As shown in Fig. 13(c), zero voltage switching (ZVS) of the switch is safely achieved at turn-on in the case of a light load. In addition, we know the ZVS operation of the Class-D inverter with the proposed control scheme is guaranteed in a whole range of variable output power. Fig. 13(d) and (e) indicate waveforms of the average output power with the proposed control scheme in the case of 100% and 10% loads.




(d) Output power $P_{out}$ at 100% load (e) Output power $P_{out}$ at 10% load

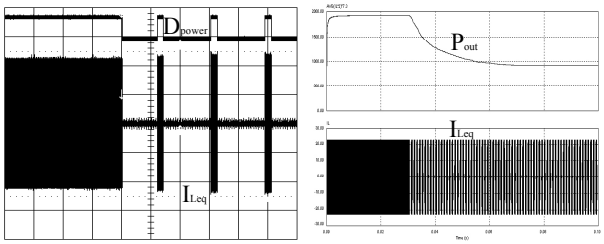
Fig. 13 The simulated and experiment result of Proposed Class-D inverter

Fig. 14(a) indicates waveforms of the average output power and load current, $I_{Leq}$ by variation of the duty cycle (form 10% to 100% load) and Fig. 14(b) indicates waveforms of the average output power and load current, $I_{Leq}$ by variation of the duty cycle (form 100% to 10% load).




(a) (10A/div., time: 0.1s)
Output power $P_{out}$ and Load current $I_{Leq}$.(from 0.1 to 1 duty cycle)
(Simulation result (right) : 10A/div., time: 0.02s $D_{power}$ : 1kHZ)

From this result, it is shown that the output power of the proposed inverter is precisely regulated in a whole load range by adjusting $D_{power}$. Also, all the experimental results are in accordance with the simulated results.




(b) (10A/div., time: 0.1s)
Output power $P_{out}$ and Load current $I_{Leq}$.(from 1 to 0.1 duty cycle)
(Simulation result (right) 10A/div., time: 0.02s $D_{power}$ : 1kHZ)

Fig. 14 Waveforms at variations of $D_{power}$.

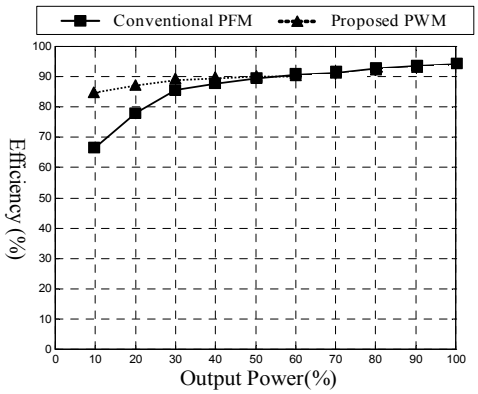



Fig. 15 Inverter efficiency comparison between the proposed PWM and the conventional PFM control scheme

Fig. 15 is the inverter efficiency curve in load range. As shown in Fig. 15, at full load, the efficiency of the Class-D inverter is the same between the conventional PFM and

the proposed PWM control scheme. But efficiency of the Class-D inverter with the proposed PWM control scheme is remarkably higher than conventional PFM Class-D inverters at light load because the ZVS is broken in cases of Class-D inverters with a conventional PFM control scheme. Therefore, the Class-D inverter with the proposed PWM control scheme has a better performance in total efficiency than those with the conventional PFM control scheme.

## 5. Conclusion

In this paper, we proposed a simple power control scheme for a Class-D inverter with CFVP (Constant Frequency Variable Power) for an induction heating jar which supplies current to an induction heating coil and explained the principles of the proposed control scheme in detail. The main advantage of this control scheme is the frequency does not have to vary because the output power simply can be controlled by $D_{power}$ in a whole load rage. Evidence that this power control is stable is proven in simulated and experiment results. It can be concluded that the proposed control scheme has the following advantages:

- It is more appropriate for wide power regulated ranges than conventional control of the Class-D inverter.
- The ZVS operation is guaranteed in a whole load range
- This control scheme has a simple configuration.
- Low switching losses, EMI and stresses are achieved
- It has better performance in efficiency in comparison to Class-D inverters with a conventional PFM control scheme.

Therefore, the proposed control scheme can be applied to other inverter topologies requiring well regulated output power.

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**Wonsuk Choi** was born in Seoul, Korea in 1977. He received a B.S. in electrical engineering from Soong-sil University, Seoul, Korea, in 2003 and a M.S. degree in electrical engineering from Hanyang University, Seoul, Korea, in 2005. He is currently working at Fairchild Semiconductor as an Application Engineer. His research interests are in induction heating application development, soft switched power supply topologies, power factor collection circuits and its control circuits.

**Nam-Ju Park** was born in Gyeongnam, Korea, in 1973. He received a M.S. degree in control and instrumentation engineering. from Gyeongsang National University, Jinju, Korea, in 2001, where he is currently working towards a Ph.D. degree in electrical engineering. of Hanyang University, Seoul, Korea. His primary areas of research interest include high-frequency resonant inverters, high frequency PWM DC-DC converter topology and its control circuit, soft switching techniques such as ZVS, ZCS, power factor correction circuits and electronic ballast.

**Dong-Yun Lee** was born in Chonbuk, Korea, in 1968. He received his M.S. and Ph.D. degrees in electrical engineering from Hanyang University, Seoul, Korea, in 1998, and 2003. He has also worked for the Korea Institute of Science Technology (KIST), Seoul, Korea, as a researcher. He is currently working at Samsung SDI as a Senior Researcher. His primary areas of research interest includes high-frequency PWM DC-DC converter topologies and its control circuits, soft switching techniques such as ZVS, ZCS, power factor collection circuits and electronic ballast.

**Dong-seok Hyun**(S'79-M'83-SM'91) received his B.E. and M.E. degrees in electrical engineering from Hanyang University, Seoul, Korea, in 1973 and 1978, respectively, and his Ph.D. degree in electrical engineering from Seoul National University, Seoul, Korea, in 1986.

From 1976 to 1979, he was with the Agency of Defense Development, Korea, as a researcher. He was a research associate in the department of Electrical Engineering, University of Toledo, Toledo, OH, during 1984-1985, and a visiting professor in Electrical Engineering at the Technical University of Munich, Germany, during 1988-1989. Since 1979, he has been with Hanyang University, where he is currently a professor in the Department of Electrical Engineering and Director of the Advanced Institute of Electrical Engineering and Electronics (AIEE). He is the author of more then 90 publications concerning electric machine design, high-power engineering, power electronics, and motor drives. His research interests include power electronics, digital signal processing, traction, and their control systems.

Dr. Hyun is a fellow member of IEEE Power Electronics , IEEE Industrial Elctronics, IEEE Industrial Appications, and IEEE Electron Device Societies, the Institution of Electrical Engineers(U.K.), the Korea Institution of Electrical Engineers, and the Circuit Control Society.